REMARKS

This is in response to the Office Action mailed on January 9, 2004, and the references cited therewith.

Claims 25, 28, and 29 are amended, no claims are canceled, and no claims are added; as a result, claims 1-35 are now pending in this application.

§102 Rejection of the Claims

Claims 1-8, 12-30, and 33 were rejected under 35 USC § 102(b) for anticipation by IEEE 1364. Applicant has carefully reviewed the reference, has amended claims 25, 28, and 29. Based on the amendments and the remarks below, Applicant respectfully traverses the rejection.

Applicant cannot find in IEEE 1364 all of the elements of claims 1-8, 12-30 or 33. Further, Applicant cannot find in IEEE 1364 all claim elements arranged as set forth in the claims. "Anticipation requires the presence in a single prior reference disclosure of each and every element of the claimed invention, *arranged as in the claim*." *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 221 USPQ 481, 485 (Fed. Cir. 1984) (citing *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 220 USPQ 193 (Fed. Cir. 1983)) (emphasis added).

IEEE 1364 apparently discusses various capabilities of Verilog® Hardware Description Language (HDL). These capabilities include the ability to force a net or a register to a value until the net or register is subsequently released. "Force" and "release" procedural statements, respectively, may be used for these purposes. (See IEEE 1364, Section 9.3.2, p. 105). IEEE 1364 also indicates that error messages may be displayed, citing an example of displaying an error message in conjunction with modeling a 3-bit priority encoder (See IEEE 1364, Section 9.5.2, p. 111).

However, Applicant submits that IEEE 1364 does not teach each end every claim element of claims 1-8, 12-30, and 33 arranged as they are in the claims. Further, Applicant's claims are distinguishable from IEEE 1364 in that Applicant's claims include at least the following distinguishing language:

- simultaneously executing at least one behavior module, which is linked to the first circuit module . . . (claims 1-7, 8, 12-14)

- at least one behavior module, which when executed results in

  forcing an initial forced logic state (or initial node condition) on the node of at least one selectable circuit module,

  releasing the node from the forced logic state if a predetermined condition is met,

  monitoring the node after the node, and

  providing an indication, in response to the monitoring, when the node is in a preselected condition (or an undesirable state).

  (claims 1-7, 8, 12-14, 15-19, 20-23, 33)

- an HDL module comprising

  a means for forcing a logic level on a simulated circuit node;

  a means for maintaining the logic level of the simulated circuit node until a release condition is met, wherein . . . a simulation program is able to change a logic state of the simulated circuit node after the release condition is met;

  a means for monitoring the simulated circuit node after the simulated circuit node has been released; and

  a means for providing an indication, in response to the monitoring, when the simulated circuit node is in a preselected condition.

  (claims 25-27, 28-30)

Further, although IEEE 1364 describes various capabilities of Verilog HDL, these capabilities are described in conjunction with a simulation program module, and not in conjunction with a behavior module that includes the limitations of Applicant's claims.

Applicant submits that the claimed combinations and arrangements are new, useful, and non-obvious. As discussed in Applicant's disclosure, the use of Applicant's various embodiments may eliminate the need and constraints of a PLI co-simulation program to perform similar functions as are performable by the claimed methods and modules. (See Disclosure p. 5, lines 17-19). Nowhere does IEEE 1364 specifically address this issue or provide a solution, nor does IEEE 1364 disclose any of the combinations of Applicant's claims.

For these reasons, Applicant believes that IEEE 1364 does not disclose the limitations of Applicant's claims 1-8, 12-30, and 33. Accordingly, Applicant believes that these claims are in a

condition for allowance. Applicant respectfully requests that the Examiner reconsider and withdraw the rejection in light of Applicant's amendments and remarks.

§103 Rejection of the Claims

Claims 9-11, 31, 32, 34, and 35 were rejected under 35 USC § 103(a) as being unpatentable over IEEE 1364 in view of Official Notice. Applicant respectfully traverses the rejection based on the remarks below.

Claims 9-11

Claims 9-11 are dependent from claim 8, which was rejected in the Office Action under 35 U.S.C. § 102. As discussed above in response to the rejection of claim 8, Applicant believes that claim 8 is distinguishable over IEEE 1364, and more specifically, that IEEE 1364 does not disclose the limitations of claim 8. Applicant further believes that IEEE 1364 neither discloses, suggests, nor motivates the limitations of Applicant's claims 9-11.

The Office Action took Official Notice as follows:

"Official Notice is given that it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the features detailed above as to enable re-forcing a node's value if testing indicates that a node's value is unknown, because it is impossible to do analysis on a node with an unknown value." (See p. 12, section 40)

Applicant respectfully traverses this Official Notice and requests the Examiner to provide a reference that describes such an element. Absent a reference, it appears that the Examiner is using personal knowledge, so the Examiner is respectfully requested to submit an affidavit as required by 37 C.F.R. § 1.104(d)(2).

In addition, nowhere in IEEE 1364 is there a disclosure, suggestion or motivation to simultaneously execute a behavior module in conjunction with a circuit module, or several of the other limitations of Applicant's claims 9-11. Applicant respectfully requests that the Examiner provide one or more additional references that disclose, suggest or motivate Applicant's claimed limitations if the rejection is repeated.

Although IEEE 1364 describes various capabilities of Verilog HDL, IEEE 1364 (alone or in combination with the Official Notice) neither discloses, suggests, nor motivates the claimed

combinations of method elements of Applicant's claims. Applicant contends that the claimed combinations are new, useful, and non-obvious. Accordingly, Applicant believes that claims 9-11 are in a condition for allowance, and respectfully requests that the Examiner reconsider and withdraw the rejection of claims 9-11.

Claims 31, 32, 34, and 35

Applicant's claims 31, 32, 34, and 35 are distinguishable from that which is disclosed in IEEE 1364 in that Applicant's claims include numerous distinguishing limitations. The Office Action states that IEEE 1364 teaches a simulated HDL circuit device having some of the elements of Applicant's claimed combination. However, Applicant respectfully disagrees. IEEE 1364 does not disclose, suggest or motivate the claimed combinations. Although IEEE 1364 describes various capabilities of Verilog HDL, IEEE 1364 (alone or in combination with the Official Notice) neither discloses, suggests, nor motivates the claimed combinations of elements of Applicant's claims. Applicant contends that the claimed combinations are new, useful, and non-obvious.

The Office Action took official notice as follows:

- ". . . it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the features detailed above as to enable re-forcing a node's value if testing indicates that a node's value is unknown, because it is impossible to do analysis on a node with an unknown value." (claims 9, 10, 11, 34)
- ". . . it is preferable to do analysis on a node that has a derived value as opposed to one with an arbitrarily assigned value." (claims 10, 11, 34)
- ". . . it would have been obvious to one of ordinary skill in the art at the time the invention was made to create two modules, because some simple circuits have only two components of interest." (claim 31)
- ". . . it would have been obvious to one of ordinary skill in the art at the time the invention was made to have a circuit with a known state pass on its state to a linked circuit with an unknown state, because this represents the propagation of a signal in a circuit." (claims 31, 32)

- ". . . it would have been obvious to one of ordinary skill in the art at the time the invention was made to create two modules, because some simple circuits have only three components of interest." (claim 32)
- ". . . In addition, it sometimes takes time for a circuit to get defined inputs from its input circuits." (claim 34)

Applicant respectfully traverses these instances of reliance on Official Notice, and requests the Examiner to provide references that describes such elements. Absent references, it appears that the Examiner is using personal knowledge, so the Examiner is respectfully requested to submit an affidavit as required by 37 C.F.R. § 1.104(d)(2).

In addition, nowhere in IEEE 1364 is there a disclosure, suggestion or motivation to combine the substances of the Notices with the features disclosed in IEEE 1364. Applicant respectfully requests that the Examiner provide one or more additional references that disclose, suggest or motivate Applicant's claimed limitations if the rejection is repeated.

For the reasons given above, Applicant believes that claims 31, 32, 34, and 35 are in a condition for allowance, and respectfully requests that the Examiner reconsider and withdraw the rejection of claims 31, 32, 34, and 35.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney, Sherry Schumm, at (480) 688-1596 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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Date May 10, 2004

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 10 day of May, 2004.

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Signature